What is claimed is:

1. A multi-stage circuit having a first stage and a second stage, the first stage having an output switch, the second stage having an input switch in communication with the output switch, the multi-stage circuit comprising:

a bootstrap module in communication with both the output switch and the input switch, the bootstrap module being capable of applying a voltage to both the input and output switches, the applied voltage ensuring that the first and second switches remain in an on state at specified times.

2. The multi-stage circuit as defined by claim 1 wherein the input and output switches have the same phase and duty cycles.

3. The multi-stage circuit as defined by claim 1 wherein during the specified times, the applied voltage is no less than a minimum turn on voltage required to turn the first and second switches to the on state.

4. The multi-stage circuit as defined by claim 1 wherein the bootstrap module is capable of receiving an input voltage at an input, the bootstrap module having an output to provide the applied voltage, the bootstrap module including a complimentary switch that electrically communicates the input with the output.

5. The multi-stage circuit as defined by claim 4 wherein the bootstrap module includes a charge storage element, the charge storage element being capable of storing a constant voltage, the complimentary switch coupling the input with the charge storage element to produce the applied voltage at the output.

6. The multi-stage circuit as defined by claim 1 further including:

a buffer coupled with the bootstrap module.

7. The multi-stage circuit as defined by claim 1 wherein the first stage and second stage comprise a switched capacitor circuit.

8. A multi-stage switched capacitor circuit comprising:

a first stage having an output switch;

a second stage having an input switch in communication with the output switch of the first stage; and

a bootstrap module coupled between both the output switch and the input switch, the bootstrap module being capable of applying the same voltage to both the output switch and the input switch.

9. The multi-stage switched capacitor circuit as defined by claim 8 wherein the first stage also includes a feedback loop coupled with the output switch.

10. The circuit as defined by claim 9 wherein the output switch and the input switch operate with the same phase and duty cycle.

11. The circuit as defined by claim 8 further including a buffer coupled between the bootstrap module and the output switch.

12. The circuit as defined by claim 8 wherein the bootstrap module is capable of receiving an input voltage at an input, the bootstrap module having a bootstrap output to provide the applied voltage, the bootstrap module including a complimentary switch that is capable of electrically communicating the input with the bootstrap output.

13. The circuit as defined by claim 8 wherein the voltage applied to the input switch is no less than a minimum turn on voltage required to turn the input switch to the on state.

14. The circuit as defined by claim 8 wherein the wherein the first stage includes a SHA, and the second stage includes an MDAC.

15. A multi-stage switched capacitor circuit comprising:

a first stage having an output feedback loop;

a second stage having an input switch in communication with the output feedback loop of the first stage; and

means for applying a bootstrap voltage to the output feedback loop and the input switch, the bootstrap voltage maintaining the input switch in an on state during a specified time interval.

16. The circuit as defined by claim 15 wherein the applying means is coupled between the output feedback loop and the input switch.

17. The multi-stage switched capacitor circuit as defined by claim 15 wherein the output feedback loop includes an output switch, the voltage applied to the output feedback loop being applied to the output switch.

18. The circuit as defined by claim 17 wherein the output switch and the input switch operate with the same phase and duty cycle.

19. The circuit as defined by claim 15 wherein the applying means is capable of receiving an input voltage at an input, the applying means having an output to provide the applied voltage, the applying means including means for electrically communicating the input with the output.

20. The circuit as defined by claim 15 wherein the wherein the first stage includes a SHA, and the second stage includes an MDAC.

21. A bootstrap module for delivering an output voltage to a switch, the bootstrap module comprising:

an input capable of receiving an input voltage;

an output capable of delivering the output voltage, the output voltage being no less than a preselected voltage required to maintain the switch in an on state, the preselected voltage being referenced to the input voltage; and

a set of input switches between the input and output, the set of input switches being capable of alternatively communicating the input voltage with the output, the output voltage being a function of the input voltage,

the set of input switches including at least one complimentary switch.

22. The bootstrap module as defined by claim 21 further comprising a charge storage element for storing the preselected voltage, the charge storage element being in electrical communication with the set of input switches.

23. The bootstrap module as defined by claim 21 wherein the output voltage is a function of the input voltage.

24. A buffer comprising:

an input to receive an input voltage;

an output to deliver an output voltage, the output voltage being substantially equal to the input voltage;

a voltage storage element;

a first transistor and a second transistor, the second transistor coupled between the voltage storage element and the output;

a set of switches coupled between the first transistor and the voltage storage element, the set of switches alternating between a reset mode and an active mode,

when in the reset mode, the voltage storage element being charged to be substantially equal to the sum of the input voltage and a given voltage,

when in the active mode, the voltage storage element shifting the input voltage by the given voltage,

the second transistor producing a voltage drop that is substantially equal to the given voltage.

25. The buffer as defined by claim 24 wherein the first transistor is a field effect transistor having its drain node and gate node connected.

26. The buffer as defined by claim 24 wherein the second transistor is a field effect transistor, the output being coupled with the source node of the second transistor.

27. The buffer as defined by claim 24 wherein the given voltage is a negative value and the voltage drop of the second transistor is a negative voltage drop.

28. The buffer as defined by claim 24 wherein the given voltage is derived from the first transistor.